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DAVID V CARLSON
SEED INTELLECTUAL PROPERTY LAW GROUP
6300 COLUMBIA CENTER
701 5TH AVENUE
SEATTLE, WA 98104-7092

| EXAMINER | |
|---|---|
| FLANDERS, ANDREW C | |
| **ART UNIT** | **PAPER NUMBER** |
| 2615 | |

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/486,582 | GEORGE ET AL. | |
| | Examiner | Art Unit | |
| | Andrew C. Flanders | 2615 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

In view of the appeal brief filed on 20 June 2006, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below. To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

### *Claim Rejections - 35 USC § 101*

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1 – 20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1 – 20 claim a method a filter and a decoder for decoding digital audio data. However, the claims are directed toward a mathematical algorithm which is merely an abstract idea. The mathematical algorithm in claims 1 – 20 do not include a practical application by physical transformation nor do they include a practical application that produces a useful, concrete and tangible result. See the interim guidelines regarding U.S.C. 101 rejections (publicly available on www.uspto.gov)

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Claims 1 – 6, 11, 18 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Uramoto (European Patent Application 0 506 111 A2).

Regarding **Claims 1 and 11**, Uramoto discloses:

A method of decoding digital data (entire document), comprising the steps of:

-obtaining an input sequence of data elements (i.e. intermediate terms) representing encoded samples (Fig. 11 element 3 outputs intermediate terms which are then input to post processing section 7; page 12 lines 10 - 15);

preprocessing the input sequence of data elements by calculating an array of sum data and an array of difference data using selected data elements from the input sequence (i.e. post processing section 7 has the same configuration of as that of Fig. 5; the input circuit of Fig. 5, element 21 sequentially or alternately receives the intermediate terms to apply a desired combination of the terms to the add/subractors 22 and 23; the data Mi and Ni is sequentially added and subtracted as taught in on page 8 lines 25 – 32; see also page 12 lines 17 - 28);

calculating a first sequence of output values using the array of sum data (i.e. the adder 22 of post processing section 7 outputs sum data as taught on page 8 lines 29 – 30 see also page 12 lines 17 - 28);

calculating a second sequence of output values using the array of difference data (i.e. the subtactor 23 of post processing section 7 outputs difference data as taught on page 8 line 31 see also page 12 lines 17 - 28);

forming decoded signals from the first and second sequences of output values (i.e. the output of the post processing section).

Uramoto does not disclose that the input sequence represents encoded digital audio data. However, Uramoto discloses that the intermediate values are derived from digital video data; page 2. Using Uramoto to operate on digital audio data in place of digital video data would have been obvious at the time of the invention. One would

have been motivated to do so in order to process audio data at a high speed; page 2 of Uramoto.

Regarding **Claim 2**, in addition to the elements stated above regarding claim 1, Uramoto further discloses:

wherein the array of sum data is obtained by adding together respective first and second data elements from the input sequence, the first and second data elements being selected from mutually exclusive sub-sequences of the input sequence (page 12 line 20; and page 8 lines 27 – 29).

Regarding **Claim 3**, in addition to the elements stated above regarding claim 1, Uramoto further discloses:

wherein the array of difference data is obtained by subtracting respective first data elements from corresponding second data elements of the input sequence, the first and second data elements being selected from mutually exclusive subsequences of the input sequence (page 12 line 23; and page 8 lines 27 – 31).

Regarding **Claim 4**, in addition to the elements stated above regarding claim 1, Uramoto further discloses:

wherein the step of calculating an array of sum data and an array of difference data comprises dividing the input data sequence into first and second equal sized sub-sequences (page 12 lines 20 and 23), the first sub-sequence comprising the higher

order data elements (page 12 line 23) of the input sequence and the second sub-sequence comprising the low order data elements of the input sequence (page 12 line 20) (also see page 8 lines 27 – 31);

calculating the array of sum data by adding together each respective data element of the first subsequence with a respective corresponding data element of the second sub-sequence (i.e. elements form Mi are added to elements of Ni and the difference is calculated as well; page 12 lines 20 – 23 and page 8 lines 27 – 31)

and calculating the array of difference data by subtracting each respective data element of the first sub-sequence from a respective corresponding data element of the second sub-sequence (i.e. elements form Mi are added to elements of Ni and the difference is calculated as well; page 12 lines 20 – 23 and page 8 lines 27 – 31).

Regarding **Claim 5**, in addition to the elements stated above regarding claim 1, Uramoto further discloses:

wherein the step of calculating a first sequence of output values comprises performing a multiply-accumulate operation utilizing each of the sum data elements (i.e. the output of the addition and subtraction (fig. 5 element 500) is applied to a data rearranging circuit which supplies an output (fig 7A elements 500 and 501), this output is then applied to a product sum operation circuit (fig. 8 element 501))

Regarding **Claim 6**, in addition to the elements stated above regarding claim 1, Uramoto further discloses:

wherein the step of calculating a second sequence of output values comprises performing a multiply-accumulate operation utilizing each of the difference data elements (i.e. the output of the addition and subtraction (fig. 5 element 500) is applied to a data rearranging circuit which supplies an output (fig 7A elements 500 and 501), this output is then applied to a product sum operation circuit (fig. 8 element 501).

Regarding **Claim 18**, in addition to the elements stated above regarding claim 2, Uramoto further discloses:

wherein the array of difference data is obtained by subtracting respective first data elements from corresponding second data elements of the input sequence, the first and second data elements being selected from mutually exclusive subsequences of the input sequence (i.e. the subtactor selects the set of x0 and x7 to create a difference value from the sets of data of (x0, x7), (x1, x6), (x2, x5) and (x3, x4); sequences Mi and Ni in the post processing section as taught on page 12).

Regarding **Claim 19**, in addition to the elements stated above regarding claim 1, the output of the addition and subtraction (fig. 5 element 500) is applied to a data rearranging circuit which supplies an output (fig 7A elements 500 and 501), this output is then applied to a product sum operation circuit (fig. 8 element 501) (i.e. wherein the step of calculating a first sequence of output values comprises performing a multiply-accumulate operation utilizing each of the sum data elements).

**Claims 7 – 10 and 12 – 17 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Uramoto (European Patent Application 0 506 111 A2) in view of ISO Standard 11172-3.

Regarding **Claim 7**, in addition to the elements stated above regarding claim 1, Uramoto does not disclose the limitations of claim 7.

ISO discloses wherein the input sequence of data elements is derived from MPEG encoded audio data (page 41 and title), and wherein the decoded audio signals comprise pulse code modulation samples (i.e. the audio data left and righ channel outputs; page 41).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the samples of the combination in ISO's decoder. One would have been motivated to do so to make the audio decoding system of the modified Uramoto system compatible with a commonly available audio encoding standard such as the MPEG standard.

Regarding **Claim 8**, Uramoto discloses adder 22 adds the data i.e. (x0 + x7) (page 8 lines 27 – 29) and subtractor 23 subtracts the data (x0 – x7) (page 8 lines 27 – 31); which in a) calculating an array of sum data $S_{ADD}[k]$ according to

$$S_{ADD}[k] = S[k] + S[m-1-k] \qquad \text{for } k = 0, 1, \ldots(m/2-1)$$

b) calculating an array of difference data $S_{SUB}[k]$ according to

$$S_{SUB}[k] = S[k] - S[m-1-k] \qquad \text{for } k = 0, 1, \ldots(m/2-1)$$

Uramoto does not disclose the rest of the claimed limitations in claim 8. ISO discloses an inverse modified discrete cosine transform (page 36). ISO also discloses multiplying samples by this function (page 41) i.e.

c) calculating a first output audio data sample by a multiply-accumulate operation according to

$$V[2i] = V[2i] + N[i, k]*S_{ADD}[k] \quad \text{for } k = 0, 1, \ldots (m/2-1)$$

$$\text{where } N[i, k] = \cos\left[\frac{(32+2i)(2k+1)\pi}{64}\right]$$

d) calculating a second output audio data sample by a multiply-accumulate operation according to

$$V[2i+1] = V[2i+1] + N[i, k]*S_{SUB}[k] \quad \text{for } k = 0, 1, \ldots (m/2-1)$$

$$\text{where } N[i, k] = \cos\left[\frac{(32+(2i+1))(2k+1)\pi}{64}\right]$$

e) and repeating steps c) and d) for $i = 0, 1, \ldots (n/2-1)$ to obtain a full set of output data.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the samples of the combination in ISO's decoder. One would have been motivated to do so to make the audio decoding system of the modified Uramoto system compatible with a commonly available audio encoding standard such as the MPEG standard.

Regarding **Claim 9**, in addition to the elements stated above regarding claim 8, ISO discloses any number of samples from 12 – 36 (page 36).

Regarding **Claim 10**, in addition to the elements stated above regarding claim 8 ISO discloses decoding MPEG audio (page 41 and title).

Regarding **Claim 12**, in addition to the elements stated above regarding claim 11, Uramoto does not explicitly disclose the elements set forth in claim 12.

ISO discloses the use of the inverse modified discrete cosine transform to decode audio data (pages 36 and 41) which meets the limitations.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the samples of the combination in ISO's decoder. One would have been motivated to do so to make the audio decoding system of the modified Uramoto system compatible with a commonly available audio encoding standard such as the MPEG standard.

Regarding **Claim 13**, in addition to the elements stated above regarding claim 12, ISO discloses decoding MPEG audio (page 41 and title).

Regarding **Claim 14**, claim 14 is rejected under the same grounds as claims 1, 11, 12 and 13 as stated above.

Regarding **Claim 15**, in addition to the elements stated above regarding claim 14, ISO discloses wherein the means for receiving an input sequence comprises a bitsgream unpacking and decoding circuit (page 41).

Regarding **Claim 16**, in addition to the elements stated above regarding claim 14, the combination further discloses:

wherein the means for calculating an array of sum data and an array of difference data comprises a reconstruction circuit (i.e. the sum and difference operations are part of a processing circuit; pages 8 and 12; page 12 and Fig. 11).

Regarding **Claim 17**, in addition to the elements stated above regarding claim 14, Uramoto further discloses:

wherein the means for calculating a first sequence of decoded output values comprises an inverse mapping circuit (i.e. the output circuit outputs the addition and subtraction data; page 12 and Fig. 11).

Regarding **Claim 20**, in addition to the elements stated above regarding claim 9, wherein the steps of decoding are repeated for decoding a series of frames of encoded audio data in an MPEG format (i.e. the bit stream inputs a series of MPEG frames to be decoded; page 41).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew C. Flanders whose telephone number is (571) 272-7516. The examiner can normally be reached on M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571) 272-7546. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

acf

SINH TRAN
SUPERVISORY PATENT EXAMINER